REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application.

At the outset, Applicant respectfully requests that the initialed PTO Form-1449 from the IDS filed on June 20, 2003, be returned. If this IDS has not been considered, appropriate consideration thereof is respectfully requested. Further, Applicant respectfully requests that the Examiner acknowledge receipt of priority documents submitted on June 20, 2003. The present application is a continuation of PCT application PCT/JP01/11623 filed on December 28, 2001, which claims priority to Japanese Patent application JP 2000-401987 filed on December 28, 2000.

Disposition of Claims

Claims 1-21 are pending in the present application. Of these claims, claims 9-21 are withdrawn from consideration. Claim 1 is independent. The remaining claims depend, directly or indirectly, from claim 1.

Claim Amendments

Independent claim 1 has been amended by way of this reply. No new matter has been added by way of these amendments, as support for these amendments may be found, for example, on page 8, lines 15-18 of the present application. Further, dependent claims 2-8 have been amended to correct minor grammatical errors. No new matter has been added by way of these amendments.

Title

A new title is required that is clearly indicative of the invention to which the claims are directed. By way of this reply, the title has been amended to "An LSI Testing Apparatus for Testing an Electronic Device."

Objection(s)

Abstract

The abstract is objected to for using legal phraseology such as "means." By way of this reply, the abstract has been amended to remove instances of such terms. Accordingly, withdrawal of the objection is respectfully requested.

Claims 2 and 3

Claims 2 and 3 are objected to for informalities. Specifically, claim 2 is objected to for being unclear as to what "means for changing a signal level" is and what it comprises, and claim 3 is objected to for being unclear as to what "means for changing a frequency of said overlaid signal" is and what it comprises. For the reasons set forth below, this objection is respectfully traversed.

As discussed with reference to Figure 1 of the present application, in one embodiment of the present invention, the power source unit (20) may include a power source (24) for generating a source voltage and a random waveform generating unit (22) for generating overlaid signals. The overlaid signals may be overlaid on the source voltage by a summing unit. The power source unit (20) includes a means for changing the signal level of the overlaid signals. As an example, the power source unit (20) may change the signal level at every test cycle. Additionally, the power source unit (20) may include a means for changing a frequency of the overlaid signals (*see* Specification, page 18, lines 2-15). Changing the level or frequency of a signal are therefore inherent functions of the power source unit (20), which is shown in Figure 1

of the present invention. It would be clear to one skilled in the art that a power source unit or a random waveform generator therein, as discussed with reference to Figure 1 of the present application, could provide means for changing a signal level or a frequency of overlaid signals. Accordingly, withdrawal of the objection is respectfully requested.

Drawings

The drawings are objected to for not showing every feature of the invention specified in the claims. Specifically, the features of "means for changing a signal level" as recited in claim 2, "means for changing a frequency of said overlaid signal" as recited in claim 3, and "said electronic device comprises a plurality of semiconductor devices" as recited in claim 8 are referenced. As discussed above, in one exemplary embodiment of the present invention, the features recited in claims 2 and 3 are inherent parts of the power source unit (20), and, as the power source unit (20) is shown in the drawings containing a power source (24) and a random waveform generating unit (22), the above features recited in claims 2 and 3 are shown in the drawings. Further, as discussed with reference to the exemplary embodiment of the present invention shown in Figure 1 of the present application, the electronic device (12) to be tested may include a digital circuit with a plurality of semiconductor devices or a digital/analog combined circuit (*see* Specification, page 7, lines 7-9). The electronic device (12), shown in Figure 1 of the present application, may comprise a plurality of semiconductor devices. Thus, the above feature recited in claim 8 is shown in the drawings. Accordingly, withdrawal of the objection is respectfully requested.

Rejection(s) under 35 U.S.C § 102

Claims 1 and 4-8 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,246,248 issued to Yamagishi (hereinafter "Yamagishi"). Independent claim 1 has

been amended in this reply to clarify the present invention recited. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

The present invention is directed to an apparatus that tests an electronic device to identify the existence of a defect in the electronic device (such as an open circuit) and judges the quality of the electronic device. As discussed with respect to Figure 1 of the present invention, in one embodiment of the present invention, the LSI testing apparatus (100) comprises a pattern generating unit (10), a power source unit (20), a detecting unit (14), and a judging unit (16). An electronic device (12) may be tested by the LSI testing apparatus (100) (*see* Specification, page 7, lines 3-9).

The pattern generating unit (10), which supplies the electronic device (12) with a source voltage to drive semiconductor devices of the electronic device (12), generates test patterns that are provided to the electronic device (12). The power source unit (20) may include a random waveform generating unit (22) and a power source (24). In one embodiment of the present invention, the random waveform generating unit may be used to generate signals with a predetermined period that are overlaid on the source voltage with a summing unit. These overlaid signals may have a signal level and a frequency that can be changed (*see* Specification, page 8, lines 2-15).

Accordingly, amended independent claim 1 of the present invention requires, in part, a power source for supplying a source voltage of direct current to said electronic device and means for overlaying an overlaid signal with a predetermined period on said source voltage supplied to the electronic device.

Yamagichi, in contrast to the present invention fails to disclose at least the above limitations of independent claim 1 of the present application. The device tester of Yamagichi includes a tester main body (10) which includes a power supply unit (14) and a programmable

voltage generation source (13) which controls the power supply unit (14). The programmable voltage generation source (13) applies a voltage indicated by the CPU (11) to the power supply terminal of the DUT (1) via a detection resistor (3) (*see* Yamagichi, col. 4, lines 36-40). Further, as discussed with reference to col. 5, lines 37-47 of Yamagichi, the CPU (11) directs the programmable voltage generation source (13) to cause the power supply unit (14) to generate a predetermined power supply voltage to the DUT (1). The voltage is proportional to current values of the power supply current I_{dd}. Thus, the power supply unit (14) under control of the programmable voltage generation source (13) outputs a single voltage to the DUT (1). Yamagichi is completely silent with respect to overlaying a signal on a source voltage that is applied to the electronic device, as required by amended independent claim 1 of the present invention.

In view of the above, Yamagishi fails to show or suggest the present invention as recited in amended independent claim 1. Thus, amended independent claim 1 is patentable over Yamagishi. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 02008/113001).

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Respectfully submitted,

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